Amendments to the Claims:

The listing of clams will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 (canceled)

Claim 2 (currently amended): An input line card comprising the apparatus of claim 1 claim 1.

Claim 3 (currently amended): The apparatus of elaim 1 claim 5, wherein the one or more state data structures maintains an indication of one of at least three different states for each of the plurality of outputs of the packet switching system.

Claim (currently amended): The apparatus of claim 3, An apparatus comprising:

a plurality of rate monitors to measure the rate at which traffic arrives for each of a plurality of outputs of a packet switching system;

one or more state data structures indicating a state of each of the plurality of outputs of the packet switching system; and

a rate-controlled virtual output queue for each of the plurality of outputs of the packet switching system, each of the rate controlled virtual output queues adjusting a rate at which packets are sent to a particular destination based at least in part on a measured traffic arrival rate and a state for the particular destination;

wherein the one or more state data structures maintains an indication of one of at least three different states for each of the plurality of outputs of the packet switching system; and

wherein packets are not sent to a particular output when the particular output is in a first state, packets are sent to the particular output at approximately the measured traffic arrival rate when the particular output is in a second state, and packets are sent to the particular output at a reduced rate approximately proportional to the measured traffic arrival rate when the particular output is in a third state.

Claim & (currently amended): The apparatus of elaim 1 claim 4, wherein each of the rate-controlled virtual output queues includes a transmit list.

Claim 6 (currently amended): The apparatus of elaim 1 claim 4, wherein each rate-controlled virtual output queue includes a timing mechanism.

Claim (currently amended): The apparatus of claim 6, An apparatus comprising:

a plurality of rate monitors to measure the rate at which traffic arrives for each of a plurality of outputs of a packet switching system;

one or more state data structures indicating a state of each of the plurality of outputs of the packet switching system; and

a rate-controlled virtual output queue for each of the plurality of outputs of the packet switching system, each of the rate controlled virtual output queues adjusting a rate at which packets are sent to a particular destination based at least in part on a measured traffic arrival rate and a state for the particular destination;

wherein each rate-controlled virtual output queue includes a timing mechanism; and wherein the timing mechanism includes one or more timing wheels.

Claim 8 (currently amended): The apparatus of claim 6, An apparatus comprising:

a plurality of rate monitors to measure the rate at which traffic arrives for each of a plurality of outputs of a packet switching system;

one or more state data structures indicating a state of each of the plurality of outputs of the packet switching system; and

a rate-controlled virtual output queue for each of the plurality of outputs of the packet switching system, each of the rate controlled virtual output queues adjusting a rate at which packets are sent to a particular destination based at least in part on a measured traffic arrival rate and a state for the particular destination;

wherein each rate-controlled virtual output queue includes a timing mechanism; and wherein the rate-controlled virtual output queue comprises at least one scheduling data structure, said at least one scheduling data structure including scheduling information with a timing granularity greater than that of the timing mechanism.

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Claim 9 (original): The apparatus of claim 8, wherein said scheduling information includes a target time for sending a next packet.

Claim 16 (currently amended): The apparatus of claim 1 claim 4, wherein each of the plurality of rate monitors include one or more data structures maintaining an indication of a packet count and a reference time period.

Claim H (original): A method performed by a packet switching system, the method comprising:

receiving packets at a first component of the packet switching system, at least a subset of the received packets being destined for a second component of the packet switching system;

maintaining a state data structure indicating a state of the second component; maintaining a rate data structure reflective of an arrival rate at which packets destined for the second component are received at the first component;

sending received packets to the second component at a first rate approximately proportional to the arrival rate when the state data structure indicates the second component is in a first state: and

sending received packets to the second component at a second rate less than the first rate and greater than zero, and approximately proportional to the arrival rate when the state data structure indicates the second component is in a second state.

Claim 12 (original): The method of claim 11, wherein the first rate is approximately the arrival rate of the received packets.

10 Claim 13 (original): The method of claim 11, wherein the rate data structure includes a count of a subset of the received packets.

Claim 14 (currently amended): The method of claim 17, wherein the <u>a set of possible</u> states for the state of the second component includes an unconstrained state, an off state, and <u>a backlogged states</u> state.

Claim 15 (original): The method of claim 14, further comprising sending no received packets to the second component from the first component when the state data structure indicates the second component is in an off state.

Claim 16 (original): A method performed by a packet switching system, the method comprising:

receiving a plurality of packets, each of the received plurality of packets being destined for one or more of a plurality of outputs of the packet switching system;

measuring a traffic arrival rate for each one of the plurality of outputs of the packet switching system, the traffic arrival rate reflective of the rate at which traffic arrives for a corresponding one of the plurality of outputs of the packet switching system;

maintaining an indication of a state of said each one of the plurality of outputs of the packet switching system;

sending received packets to a particular one of the plurality of outputs at a first rate approximately proportional to the measured traffic arrival rate for the particular one of the plurality of outputs when the maintained state indication reflects the particular one of the plurality of outputs is in a first state; and

sending received packets to the particular one of the plurality of outputs at a second rate less than the first rate and greater than zero, and approximately proportional to the measured traffic arrival rate for the particular one of the plurality of outputs when the maintained state indication reflects the particular one of the plurality of outputs is in a second state.

Claim 17 (original): The method of claim 16, wherein no packets are sent to a particular one of the plurality of outputs when the maintained state indication reflects the particular one of the plurality of outputs is in a third state

Claim 18 (currently amended): The method of claim 16, where the state data structure is wherein said indications of said states of the plurality of outputs are updated based on received flow control information.

Claim 19 (original): The method of claim 16, wherein said method is performed by an input line card of the packet switching system.

Claim 20 (original): The method of claim 16, wherein measuring the traffic arrival rate includes maintaining a packet count and a time reference.

Claim 27 (original): The method of claim 16, further comprising:
maintaining a packet queue for each output of the packet switching system; and
placing each packet of the plurality of received packets in one of the plurality of packet
queues based on a destination of said each packet.

Claim 22 (original): The method of claim 21, further comprising placing an indicator of a corresponding one of the plurality of packet queues in a transmit list upon arrival of a particular received packet having a destination of a selected one of the plurality of outputs being in the first state.

Claim 23 (original): The method of claim 16, wherein sending received packets to the particular one of the plurality of outputs at the second rate includes:

sending one of the plurality of packets to the particular one of the plurality of outputs of the packet switching system; and

rescheduling the particular one of the plurality of outputs of the packet switching system in a timing data structure for a second scheduled time based upon the measured traffic arrival rate for the selected output.

Claim 24 (original): The method of claim 23, wherein sending received packets to the particular one of the plurality of outputs at the second rate includes retrieving a transmit indication corresponding to the particular one of the plurality of outputs of the packet switching system from the timing data structure at a first scheduled time.

24 Claim 25 (original): The method of claim 25, wherein the second scheduled time reflects an actual time to send one of the plurality of packets to the selected output of the packet switching system rather than a time relative to a last sent packet to the selected output of the packet switching system.

25 Claim 26 (original): The method of claim 23, wherein the timing data structure includes one or more timing wheels.

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Claim 27 (original): The method of claim 23, comprising maintaining a target time for the sending one of the plurality of packets, wherein the second scheduled time is approximately the target time.

Claim 28 (original): The method of claim 27, wherein the target time has a finer timing resolution than that of the timing data structure.

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Claim 29 (currently amended): The method of claim 16, wherein sending received packets to the particular one of the plurality of outputs at the second rate includes:

retrieving a transmit indication corresponding to a selected output of the plurality of outputs of the packet switching system from a timing data structure at a first scheduled time and placing the placing the retrieved transmit indication in a transmit list;

removing the retrieved transmit indication from the transmit list and sending one of the plurality of packets to the corresponding selected output of the plurality of outputs of the packet switching system based on the retrieved transmit indication; and

rescheduling the sending one of the plurality of packets to the corresponding selected output of the plurality of outputs of the packet switching system in the timing data structure for a second scheduled time based upon the measured traffic arrival rate for the selected output.

Claim 36 (original): The method of claim 29, wherein the rescheduling process occurs after the transmit indication is removed from the transmit list.

Claim 27 (original): The method of claim 29, wherein the second scheduled time reflects an actual time to send one of the plurality of packets to the selected output of the packet switching system rather than a time relative to a last sent packet to the selected output of the packet switching system.

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Claim 22 (original): A packet switch system, comprising:

means for receiving packets at a first component of the packet switching system, at least a subset of the received packets being destined for a second component of the packet switching system;

means for maintaining a state data structure indicating a state of the second component;

means for maintaining a rate data structure reflective of an arrival rate at which packets destined for the second component are received at the first component;

means for sending received packets to the second component at a first rate approximately proportional to the arrival rate when the state data structure indicates the second component is in a first state; and

means for sending received packets to the second component at a second rate less than the first rate and greater than zero, and approximately proportional to the arrival rate when the state data structure indicates the second component is in a second state.

Claim 33 (original): The packet switch system of claim 32, wherein the first rate is approximately the arrival rate of the received packets.

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Claim 34 (original): The packet switch system of claim 32, wherein the rate data structure includes a count of a subset of the received packets.

Claim 35 (currently amended): The packet switch system of claim 32, wherein the a set of possible states for the state of the second component includes an unconstrained state, an off state, and a backlogged states state.

Claim 36 (original): The packet switch system of claim 35, further comprising means for sending no received packets to the second component from the first component when the state data structure indicates the second component is in an off state.

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Claim 37 (original): A machine-readable medium having stored thereon data representing sequences of instructions, said sequences of instructions which, when executed by a processor, cause said processor to perform the following:

receiving packets at a first component of the packet switching system, at least a subset of the received packets being destined for a second component of the packet switching system;

maintaining a state data structure indicating a state of the second component: maintaining a rate data structure reflective of an arrival rate at which packets destined for the second component are received at the first component;

sending received packets to the second component at a first rate approximately proportional to the arrival rate when the state data structure indicates the second component is in a first state; and

sending received packets to the second component at a second rate less than the first rate and greater than zero, and approximately proportional to the arrival rate when the state data structure indicates the second component is in a second state.

Claim 28 (currently amended): The machine readable medium of claim 27, wherein the a set of possible states for the state of the second component include includes an unconstrained state, an off state, and a backlogged states state.

Claim 39 (original): The machine readable medium of claim 38, wherein said processor further performs sending no received packets to the second component from the first component when the state data structure indicates the second component is in an off state.